

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

HEA-SUK JUNG

Application No.:

Filed:

For: **delay locked loop (dll) in semiconductor device**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

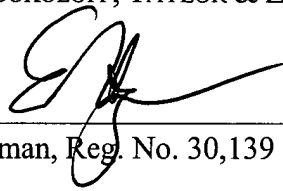
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Date: 8/5/03

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP


Eric S. Hyman, Reg. No. 30,139

12400 Wilshire Blvd., 7th Floor
Los Angeles, California 90025
(310) 207-3800

Information Disclosure Statement

New U.S. Patent Application for
DELAY LOCKED LOOP (DLL) IN SEMICONDUCTOR DEVICE
Our Ref. No.: P03H1037/US/wy

Reference No.:

- (1) US Patent No. 6,552,955
- (2) US Patent No. 6,492,852
- (3) US Patent No. 6,075,395
- (4) US Publication No. 2003/0085744 A1
- (5) US Publication No. 2003/0081491 A1
- (6) US Publication No. 2003/0001637 A1
- (7) JP Laid-Open No. 2001-283589
- (8) JP Laid-Open No. 2000-100163
- (9) JP Laid-Open No. 11-259167
- (10) JP Laid-Open No. 11-214986
- (11) JP Laid-Open No. 11-72540